CLAIMS

What is claimed is:

1. A semiconductor device having a bonding pad electrode of a multi-layer structure, said semiconductor device comprising:

a semiconductor substrate;

a lower electrode layer formed on said semiconductor substrate;

a cover insulating film formed on said lower electrode layer, wherein said cover insulating film has an opening for exposing at least a portion of said lower electrode layer, a step portion is provided at a side wall of said opening of said cover insulating film, the size of said opening at the upside portion of a step surface of said step portion is larger than the size of said opening at the downside portion of said step surface; and

an upper electrode layer formed on said portion of said lower electrode layer exposed via said opening, said upper electrode layer being made of material having corrosion resistance against substance which is corrosive to said lower electrode layer, and said upper electrode layer overlaps said step surface of said step portion.

2. A semiconductor device as set forth in claim 1, wherein said cover insulating film comprises a silicon nitride film and a PSG (phospho silicate glass) film formed on said silicon nitride film, said step surface of said step portion being a surface portion of said silicon nitride film.

3. A semiconductor device as set forth in claim 1, wherein said

cover insulating film comprises a PSG film.

4. A semiconductor device as set forth in claim 1, wherein said lower electrode layer comprises a metal film containing aluminum, and said upper electrode layer comprises a metal film which has corrosion resistance against substance corrosive to aluminum.

5. A semiconductor device as set forth in claim 4, wherein said upper electrode layer comprises a TiNiAg film.

6. A semiconductor device as set forth in claim 1, further comprising a high conductivity metal plate coupled onto said upper electrode layer via a conductive paste.

7. A semiconductor device as set forth in claim 6, wherein said conductive paste is an Ag paste, and said metal plate is a copper plate.

8. A semiconductor device as set forth in claim 6, wherein said bonding pad electrode is a source pad electrode of a power MOSFET.

9. A semiconductor device as set forth in claim 1, wherein said bonding pad electrode is a source pad electrode of a MOSFET.

10. A method of manufacturing a semiconductor device having a bonding pad electrode of a multi-layer structure, said method comprising:

preparing a semiconductor substrate;

forming a lower electrode layer on said semiconductor substrate;

forming a cover insulating film on said lower electrode layer;

forming an opening in said cover insulating film to expose at least a portion of said lower electrode layer, wherein a step portion is provided at a side wall of said opening of said cover insulating film, the size of said opening at the upside portion of a step surface of said step portion is larger than the size of said opening at the downside portion of said step surface; and

forming an upper electrode layer on said portion of said lower electrode layer exposed via said opening, wherein said upper electrode layer being made of material having corrosion resistance against substance which is corrosive to said lower electrode layer, and said upper electrode layer overlaps said step surface of said step portion.

11. A method of manufacturing a semiconductor device as set forth in claim 10, wherein said forming an opening in said cover insulating film to expose at least a portion of said lower electrode layer comprises:

forming a photo resist film having a first opening on said cover insulating film; and

isotropically etching said cover insulating film by using said photo resist film as an etching mask, wherein said cover insulating film is side-etched with respect to said first opening of said photo resist film;

wherein said forming an upper electrode layer on said portion of said lower electrode layer exposed via said opening is

performed by using a lift-off method in which said photo resist film is used as a mask.

12. A method of manufacturing a semiconductor device as set forth in claim 10, wherein said cover insulating film comprises a silicon nitride film and a PSG film;

wherein said forming said cover insulating film on said lower electrode layer comprises:

forming said silicon nitride film on said lower electrode layer; and

forming said PSG film on said silicon nitride film;

wherein said forming an opening in said cover insulating film to expose at least a portion of said lower electrode layer comprises:

forming a photo resist film having a first opening on said PSG film;

isotropically etching said PSG film by using said photo resist film as an etching mask to form a second opening in said PSG film, wherein at least a portion of said silicon nitride film is exposed at the bottom portion of said second opening, and said PSG film is side-etched with respect to said first opening of said photo resist film; and

plasma etching said silicon nitride film by using said photo resist film as an etching mask to form a third opening in said silicon nitride film, wherein at least a portion of said lower electrode layer is exposed at the bottom portion of said third opening, said third opening is smaller than said second opening, and said step surface of said step portion is formed by the upper surface portion of said silicon nitride film exposed via said second opening of said PSG film; and

wherein said forming an upper electrode layer on said portion of said lower electrode layer exposed via said opening of said cover insulating film comprises:

depositing a material to be said upper electrode layer on said exposed portion of said lower electrode layer, at least a portion of said step surface and said photo resist film; and

removing a portion of said material deposited on said photo resist film by using a lift-off method, wherein portions of said material deposited on said exposed portion of said lower electrode layer and on said step portion are not removed, thereby said upper electrode layer is formed.

13. A method of manufacturing a semiconductor device as set forth in claim 10, wherein said cover insulating film comprises a silicon nitride film and a PSG film;

wherein said forming said cover insulating film on said lower electrode layer comprises:

forming said silicon nitride film on said lower electrode layer;

forming a first photo resist film having a first opening on said silicon nitride film; plasma etching said silicon nitride film by using said first photo resist film as an etching mask to form a second opening in said silicon nitride film;

removing said first photo resist film; and

forming said PSG film on said silicon nitride film so as to fill said second opening of said silicon nitride film;

wherein said forming an opening in said cover insulating film to expose at least a portion of said lower electrode layer comprises:

forming a second photo resist film having a third opening

on said PSG film, wherein said third opening is larger than said second opening; and

isotropically etching said PSG film by using said second photo resist film as an etching mask to form a fourth opening in said PSG film, wherein said PSG film is side-etched with respect to said third opening of said second photo resist film, said fourth opening is larger than said second opening, at least a portion of said lower electrode layer is exposed via said second and fourth openings, and the upper surface portion of said silicon nitride film exposed via said fourth opening of said PSG film forms said step surface of said step portion;

wherein said forming an upper electrode layer on said portion of said lower electrode layer exposed via said opening of said cover insulating film comprises:

depositing a material to be said upper electrode layer on said exposed portion of said lower electrode layer, at least a portion of said step surface and said photo resist film; and

removing a portion of said material deposited on said second photo resist film by using a lift-off method, wherein portions of said material deposited on said exposed portion of said lower electrode layer and on said step surface are not removed, thereby said upper electrode layer is formed.

14. A method of manufacturing a semiconductor device as set forth in claim 10, wherein, in said forming said cover insulating film on said lower electrode layer, a PSG (phospho silicate glass) film is formed as said cover insulating film on said lower electrode layer;

wherein said forming an opening in said cover insulating film to expose at least a portion of said lower electrode layer

comprises:

forming a first photo resist film having a first opening on said PSG film;

etching said PSG film by using said first photo resist film as an etching mask to form a trench in said PSG film, wherein, in the bottom portion of said trench, said lower electrode layer is not exposed;

removing said first photo resist film;

forming a second photo resist film having a second opening on said PSG film, wherein said second opening is larger than the size of said trench; and

isotropically etching said PSG film by using said second photo resist film as an etching mask to expose at least a portion of said lower electrode layer at the bottom portion of said trench, wherein said PSG film is side-etched with respect to said second opening of said second photo resist film, and said step surface of said step portion is formed at the side surface of said exposed PSG film;

wherein said forming an upper electrode layer on said portion of said lower electrode layer exposed via said opening of said cover insulating film comprises:

depositing a material to be said upper electrode layer on said exposed portion of said lower electrode layer, at least a portion of said step surface and said second photo resist film; and

removing a portion of said material deposited on said second photo resist film by using a lift-off method, wherein portions of said material deposited on said exposed portion of said lower electrode layer and on said step surface are not removed, thereby said upper electrode layer is formed.

15. A method of manufacturing a semiconductor device as set forth in claim 10, wherein said lower electrode layer comprises a metal film containing aluminum, and said upper electrode layer comprises a metal film which has corrosion resistance against substance corrosive to aluminum.

16. A method of manufacturing a semiconductor device as set forth in claim 15, wherein said upper electrode layer comprises a TiNiAg film.

17. A method of manufacturing a semiconductor device as set forth in claim 10, further comprising: coupling a high conductivity metal plate onto said upper electrode layer via a conductive paste, after forming said upper electrode layer on a portion of said lower electrode layer exposed via said opening.

18. A method of manufacturing a semiconductor device as set forth in claim 17, wherein said conductive paste is an Ag paste, and said metal plate is a copper plate.

19. A method of manufacturing a semiconductor device as set forth in claim 17, wherein said bonding pad electrode is a source pad electrode of a power MOSFET.

20. A method of manufacturing a semiconductor device as set forth in claim 10, wherein said bonding pad electrode is a source pad electrode of a MOSFET.